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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
Hirohisa SUZUKI of Gunma-ken, Japan and Masaaki TAIRA of Hyougo-ken, Japan
Serial No: Not assigned
Filed: June 26, 2000
For: NOISE CANCEL CIRCUIT

Box PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Transmitted herewith for filing is the patent application identified above.

- ☒ 5 sheet(s) of drawings (☒ formal ☐ informal) is(are) enclosed.
- ☒ 11 page(s) of specification and 1 page(s) of abstract of the invention are enclosed.
- ☐ An assignment of the invention to SANYO ELECTRIC CO., LTD. ☐ is enclosed ☒ will follow.
- ☐ An associate power of attorney ☐ is enclosed ☐ will follow.
- ☐ A verified statement to establish small entity status under 37 C.F.R. §§ 1.9 & 1.27 is enclosed.
- ☐ Declaration and Power of Attorney ☐ is enclosed ☒ will follow.
- ☐ A certified copy of Japanese Patent Application No. 11-184029 filed June 29, 1999 from which priority is claimed under 35 U.S.C. § 119 will follow.
- ☐ IDS enclosed (☐ with references).
- ☐ Preliminary Amendment is enclosed.

**CALCULATION OF FEES**

| | ITEM | TOTAL NO. OF CLAIMS | | NO. OF CLAIMS OVER BASE | LG/SM $ ENTITY FEE | | $ AMOUNT | $ FEE |
|---|---|---|---|---|---|---|---|---|
| A | TOTAL CLAIMS FEE | 9 | -20 | 0 | LG=$18 SM=$9 | $18 | 0 | |
| B | INDEPENDENT CLAIMS FEE* | 1 | -3 | 0 | LG=$78 SM=$39 | $78 | 0 | |
| C | SUBTOTAL - ADDITIONAL CLAIMS FEE (ADD FINAL COLUMN IN LINES A + B) | | | | | | | $ 0 |
| D | MULTIPLE-DEPENDENT CLAIMS FEE | | | | | LARGE ENTITY FEE = $260 SMALL ENTITY FEE = $130 | | $ 0 |
| E | BASIC FEE | | | | | LARGE ENTITY FEE = $690 SMALL ENTITY FEE = $345 | | $ 690 |
| F | TOTAL FILING FEE (ADD TOTALS FOR LINES C, D, AND E) | | | | | | | $ 690 |
| G | ASSIGNMENT RECORDING FEE | | | | | | $ 40 | $ 40 |
| | *LIST INDEPENDENT CLAIMS 1. | | | | | | | |

"Continued on Second Page"

☐ A check in the amount of $ 0 to cover the filing fee is enclosed.

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Please associate this application with the attorneys of record and with the correspondence address recorded for Customer No. 22335.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: June 26, 2000

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Hirohisa SUZUKI, et al.

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Art Unit: Not assigned

Examiner: Not assigned



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Dear Sir:

I hereby certify that

- ☒ two copies of a letter of transmittal
- ☒ patent application (__11__ page(s) of specification; __9__ claim(s); __1__ page(s) of abstract
- ☒ __5__ sheet(s) of formal drawings
- ☒ return postcard

are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service with sufficient postage under 37 C.F.R. § 1.10 on the date indicated above and are addressed to:

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Date: June 26, 2000

Tommy Mitchell
Name of person mailing papers

Signature

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# NOISE CANCEL CIRCUIT

## BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a noise cancel circuit which removes noise using an interpolation technique.

2. Description of the Background Art

Generally, when a pulse noise generated by a vehicle engine overlaps with the audio band, a car radio receiver will produce an audible noise unpleasant to listeners. To prevent this, radio receivers usually include a noise cancel circuit. Such a noise cancel circuit removes a pulse noise from an audio signal by performing pre-hold processing on the signal during noise generation. A conventional noise cancel circuit is shown in Fig. 3.

In Fig. 3, an input signal including noise is supplied via the input terminal 31 to the delay circuit 32 and HPF 33. After passing through the HPF 33, if noise exceeding a certain predetermined level is detected by the noise detection circuit 34, the noise detection circuit 34 produces an output pulse. The output pulse in applied to the gate generation circuit 35, which generates a gate signal having a predetermined width.

In response to the gate signal, the switch 36 is turned off. As a result, application of a pilot cancel signal to the subtraction circuit 37 is stopped, thereby allowing the output signal from the delay circuit 32 to be supplied to both input terminals of the subtraction circuit 37. The output AC signal from the delay circuit 32 is canceled by the subtraction circuit, and the DC

voltage between the two ends of the capacitor 38 results at the output end of the subtraction circuit 38. The delay time of the delay circuit 32 equals the time required for the processing from the HPF 33 to the switch 36. In this way, noise within the input signal is removed. Subsequently, when the gate signal generation is stopped, the switch 36 is turned on, and the pilot cancel signal is applied to the subtraction circuit 37. The pilot signal component within the input signal is then canceled by the subtraction circuit 37.

However, as the frequency band of noise such as pulse noise is often within the audio frequency band, the noise removal by pre-hold processing removes not only noise, but also sound. While noise removal by pre-hold processing may produce an output that sounds improved to the ear, the pre-hold processing also actually decreases the distortion factor, thereby newly introducing deterioration of sound quality.

## SUMMARY OF THE INVENTION

The object of the present invention is to provide a noise cancel circuit for removing noise, such as pulse noise, from an audio signal while minimizing decrease in the distortion factor.

According to the present invention, during pulse noise generation, interpolation is performed on the noise portion of a detected radio signal. As a result, the noise portion is interpolated to a smooth curve, and the distortion factor of the detected radio signal can be improved.

## BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram illustrating an embodiment of the

present invention.

Fig. 2 is a characteristic diagram for explaining the operation according to the present invention.

Fig. 3 is a block diagram showing a conventional example.

Fig. 4 is a block diagram illustrating a specific configuration example of the interpolation circuit 4 in Fig. 1.

Fig. 5 is a flowchart for explaining the operation according to Fig. 4.

Fig. 6 is a diagram for explaining the timing of pulse removal.

Fig. 7 is another diagram for explaining the timing of pulse removal.

## DESCRIPTION OF THE PREFERRED EMBODIMENT

Fig. 1 is a block diagram illustrating a preferred embodiment of the present invention. Numerals 1 and 2 denote delay circuits which are supplied with a signal such as a detected FM signal. 3 is an LPF which passes only a predetermined band within the output signal from delay circuit 2. 4 is an interpolation circuit for interpolating a data of a time point using data of previous and later time points. 5 denotes an AGC amplifier which detects the magnitude of white noise and performs amplification while suppressing the white noise level. 6 is a noise detection circuit for detecting pulse noise in the output signal from the AGC amplifier 5. 7 is a timer for counting during a predetermined time period T according to the output signal from the noise detection circuit 6, and generating an output signal during the counting. 8 denotes a selection circuit for selecting an output signal from either the delay circuit 1 or the interpolation circuit 4 depending

on the presence of the output signal from the timer 7.

In a device employing the arrangement of Fig. 1, a detected FM signal is supplied to three circuits. In delay circuit 1, the detected FM signal is delayed by delay time $\tau 1$ and supplied to one of the input terminals of the selection circuit 8. In delay circuit 2, the detected FM signal is delayed by delay time $\tau 2$ and supplied to the LPF 3. When the detected FM signal is an FM composite signal, for example, the LPF 3 blocks the sub-signal and the pilot signal by reducing their levels, and allowing only the main signal to be passed. The output signal from the LPF 3 is applied to the interpolation circuit 4 for interpolation processing. By applying only the main signal to the interpolation circuit 4, erroneous processing due to sub-signals and pilot signals is prevented. The interpolation circuit 4 may be configured using a DSP or a logic circuit as shown in Fig. 4, and may comprise an A/D converter 41 for converting the output from the LPF 3 into digital data, an arithmetic unit 42 for performing interpolation processing on the output data from the A/D converter 41, a D/A converter 43 for converting the output from the arithmetic unit 42 into an analog signal, and a memory 44 for storing audio data. For the interpolation processing, spline interpolation, especially Lagrange interpolation, is performed. The interpolation circuit 4 constantly performs the interpolation processing to produce an analog interpolation signal which is supplied to the other of the input terminals of the selection circuit 8.

Further, the detected FM signal is applied to the AGC amplifier 5. When the white noise level is high, the AGC amplifier amplifies the detected FM signal while reducing the gain such that

the white noise level becomes suppressed. The output signal from the AGC amplifier is supplied to the noise detection circuit 6. The noise detection circuit 6 extracts and detects the pulse noise components. The detection output signal from the noise detection circuit 6 is applied to the timer 7. The counting operation of the timer 7 is started in response to the input of the detection signal. The timer 7 counts during a predetermined time period T, and generates an output signal during the counting. In response to this output signal, the selection circuit 8 selects the output signal from the interpolation circuit 4 as shown in Fig. 1.

In the arrangement of Fig. 1, when no pulse noise component is detected within the input audio signal, the noise detection circuit 6 generates no output signal. As a result, the selection circuit 8 indicates a state opposite from that shown in Fig. 1, and the audio signal output from delay circuit 1 is transmitted, via the selection circuit 8, to the circuitry of the next stage. When pulse noise components are generated, the selection circuit 8 selects the output signal from the interpolation circuit 4, allowing a signal subjected to interpolation processing in its noise portions to be transmitted to the circuitry of the next stage.

Each of the raw input signal line, the interpolation circuit line, and the noise detection line require different processing time periods. Accordingly, noise cannot be appropriately removed if the processes in those lines are performed without delaying the signals. Delay circuits 1 and 2 are therefore provided to make timing adjustments such that appropriate noise removal can be accomplished.

An example case is described below in which a pulse noise is generated at time t0 as shown in Fig. 6. The noise detection

circuit 6 detects the pulse noise by detecting a change in the input signal level. The noise detection circuit 6 usually conducts pulse noise detection based on the state of change in the data obtained after performing A/D conversion, thus requiring time for such processing. Because the time point of pulse noise detection is always later than that of the noise generation, and also because performing processing for detection requires a certain amount of time, the time point that the noise detection output signal is generated from the actual noise detection circuit 6 is t1. Delay time $\tau 1$ of delay circuit 1 may be designated to correspond to the period of time between time point t1 of the output signal generation from the noise detection circuit 6 and time point t0 of the pulse generation. With this arrangement, the selection circuit 8 can be switched at a timing matching the pulse generation. In the interpolation circuit 4, processing time is similarly required because D/A conversion and interpolation processing are executed. Assuming that the time required for interpolation processing is $\tau a$, delay time $\tau 2$ of delay circuit 2 may be designated as follows: $\tau 2 = \tau 1 - \tau a$ ($\tau 1 = \tau 2 + \tau a$). According to this arrangement, an interpolation output corresponding to the noise generation time point t1 is supplied from the interpolation circuit 4 via the selection circuit 8 at the timing when the selection circuit 8 is switched. In this way, the timing of the interpolation output is also matched. It should be noted that, in Fig. 6, the timing is illustrated diagrammatically without accurately reflecting the actual scale of the timing. The count time T of the timer 7 is generally set at the pulse width of the pulse noise. Accordingly, the interpolation output from the interpolation circuit 4 is supplied from the selection circuit 8 during a time period

corresponding to the generation of the pulse.

Delay time $\tau 2$ is further explained with reference to Fig. 7. In Fig. 7, the processing times of the noise detection circuit 6 and the interpolation circuit 4 are assumed to be 0. Furthermore, the signal forward direction in Fig. 7 is the opposite from Fig. 6.

The noise detection circuit 6 detects a pulse noise at the peak of the noise. If delay circuit 2 is not provided in the interpolation line including the interpolation circuit 4, the latter, not the former, half of the pulse noise can be removed when the selection circuit 8 is switched at the timing of the peak. By inserting delay circuit 2, all pulse noise can be removed. It is to be noted that, in comparison with the detection processing time of the noise detection circuit 6, the interpolation processing time of the interpolation circuit 4 is longer. Accordingly, when taking into account the processing times of both of the circuits, delay time $\tau 2$ of delay circuit 2 may be designated shorter than the time period indicated in Fig. 7 by the time period difference between the interpolation processing time and the detection processing time.

The operation of the interpolation circuit 4 is next described referring to Fig. 4. The output data from the A/D converter circuit 41 is transmitted to the arithmetic unit 42 and sequentially stored in the memory 44. The data read out from the memory 44 is used to calculate interpolation data by spline or Lagrange interpolation. The output interpolation data is converted into an analog data by the D/A converter circuit 44 and supplied to the selection circuit 8 in Fig. 1.

The processing of the arithmetic unit 42 is explained using

the flowchart of Fig. 5. With respect to the data to be interpolated, data for three points from previous and later time points, respectively, are read out (S1). Subsequently, interpolation data is calculated using a Lagrange interpolation technique. For example, when point X in Fig. 2 is to be interpolated, data of previous and later time points, data x0 to data x5, and their function values f0 to f5, are read out according to S1. The read out data are substituted in the following equation:

$$P(x) = \sum_{k=0}^{n} L_k(x) f_k \tag{1}$$

$L_k(x)$ is the Lagrange interpolation coefficient, which can beexpressed as

$$L_k(x) = \frac{(x-x_0)(x-x_1)\cdots(x-x_{k-1})(x-x_{k+1})\cdots(x-x_n)}{(x_k-x_0)(x_k-x_1)\cdots(x_k-x_{k-1})(x_k-x_{k+1})\cdots(x_k-x_n)} \tag{2}$$

Using the example of Fig. 2, the function value f(x) to be interpolated is given by

$$P(x) = L(0)f0 + L(1)f1 + L(2)f2 + L(3)f3 + L(4)f4 + L(5)f5 \tag{3}$$

and can be calculated by substituting the read out data. In this case, the Lagrange interpolation coefficient is

$$Lk(x) = \frac{(x-x0)(x-x1)(x-x2)(x-x3)(x-x4)(x-x5)}{(xk-x0)(xk-x1)(xk-x2)(xk-x3)(xk-x4)(xk-x5)} \tag{4}$$

According to this Lagrange interpolation, a smooth curve passing through all given points, points x0 to x5 in Fig. 2, can be obtained. By performing interpolation using this technique, the noise portion

of the raw signal can be interpolated into a smooth curve, allowing improvement of the distortion factor.

The calculated value is output from the arithmetic unit 42 (S3), and then the next interpolation data, namely, the interpolation data which corresponds to f3 in Fig. 2, is calculated. The arithmetic unit sequentially calculates interpolation data based on the data stored in the memory 44.

Although Lagrange interpolation is used in the interpolation circuit 4 of the present embodiment to calculate the interpolation value, other interpolation techniques may be used for the calculation of the present invention. Furthermore, a plurality of interpolation techniques may be employed in combination such that the optimal interpolation technique can be selected to calculate the interpolation value according to the condition of noise generation.

According to the present invention, noise portions can be smoothly interpolated by spline interpolation. Sound components are therefore prevented from being deleted by noise removal, allowing further improvement of the distortion factor and sound quality.

What is claimed is:

1. A noise cancel circuit for removing noise components in a detected radio signal, comprising:

an interpolation circuit for performing interpolation processing on said detected radio signal, wherein

during generation of a pulse noise, a noise portion of said detected radio signal is interpolated by an output signal from said interpolation circuit.

2. The noise cancel circuit defined in Claim 1, wherein

said interpolation circuit executes spline interpolation.

3. The noise cancel circuit defined in Claim 1, further comprising:

a noise detection circuit for detecting the noise portion of said detected radio signal, wherein

the noise portion of said detected radio signal is interpolated by said interpolation circuit according to an output signal from said noise detection circuit.

4. The noise cancel circuit defined in Claim 3, further comprising:

a selection circuit for selecting either the output signal from said interpolation circuit or said detected radio signal, wherein

said selection circuit is controlled according to the output signal from said noise detection circuit.

5. The noise cancel circuit defined in Claim 4, wherein said interpolation circuit performs interpolation processing and outputs an interpolation signal regardless of presence or absence of noise components.

6. The noise cancel circuit defined in Claim 5, further comprising:

a first delay circuit for delaying said detected radio signal and supplying the delayed signal to said selection circuit; and

a second delay circuit for delaying said interpolation signal from said interpolation circuit.

7. The noise cancel circuit defined in Claim 6, wherein said second delay circuit is disposed in a processing stage prior to said interpolation circuit.

8. The noise cancel circuit defined in Claim 6, wherein a delay time of said first delay circuit corresponds to a sum of an interpolation processing time of said interpolation circuit and a delay time of said second delay circuit.

9. The noise cancel circuit defined in Claim 8, wherein the delay time of said second delay circuit corresponds to a difference obtained by subtracting the interpolation processing time of said interpolation circuit from a time delay between generation and detection of said pulse noise.

## ABSTRACT OF THE DISCLOSURE

A raw signal is delayed in a delay circuit (1) and then supplied to one of the input terminals of a selection circuit (8). The raw signal is also supplied to another delay circuit (2) to be delayed. Subsequently, data of this delayed signal is processed by spline interpolation in an interpolation circuit (4), and the interpolation values are supplied to the other of the input terminals of the selection circuit (8). Further, a timer (7) is operated according to an output signal from a noise detection circuit (6) which detects noise in the raw signal. When noise is detected, the selection circuit (8) switches to select the output from the interpolation circuit (4), thereby achieving interpolation of noisy sections.

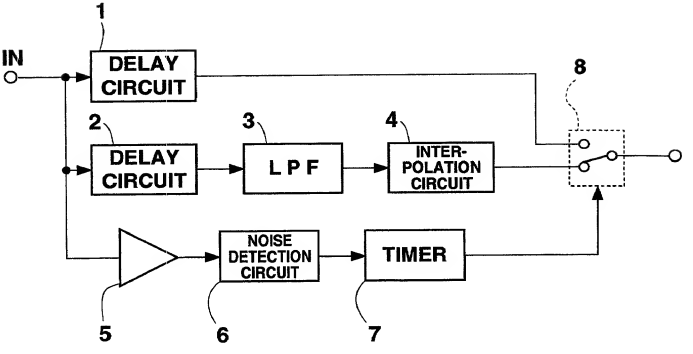
IN
1
DELAY CIRCUIT
2
DELAY CIRCUIT
3
L P F
4
INTER-POLATION CIRCUIT
8
NOISE DETECTION CIRCUIT
TIMER
5
6
7

Fig. 1

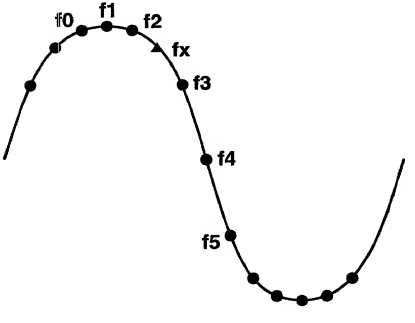
f0
f1
f2
fx
f3
f4
f5

Fig. 2

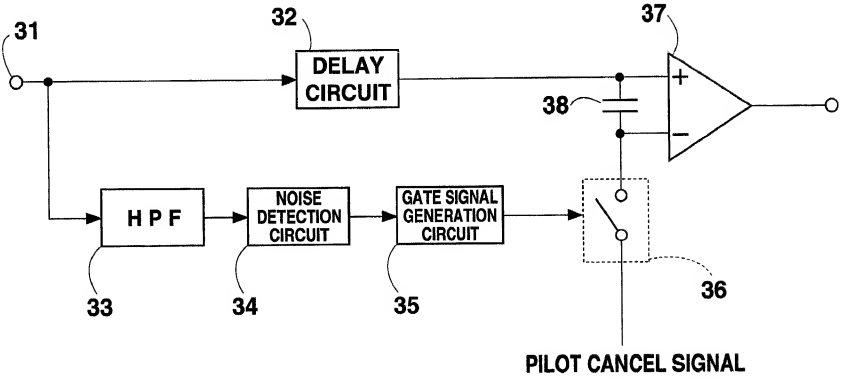


Fig. 3 PRIOR ART

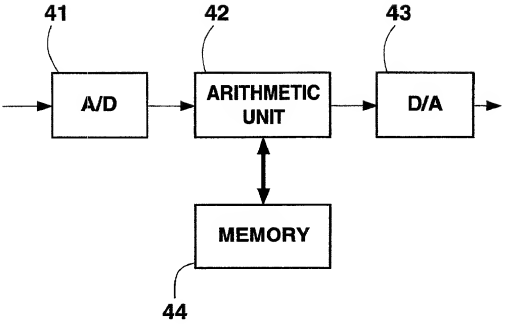
41
42
43
A/D
ARITHMETIC UNIT
D/A
MEMORY
44

Fig. 4

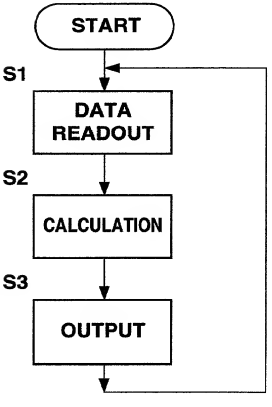
START
S1
DATA READOUT
S2
CALCULATION
S3
OUTPUT

Fig. 5

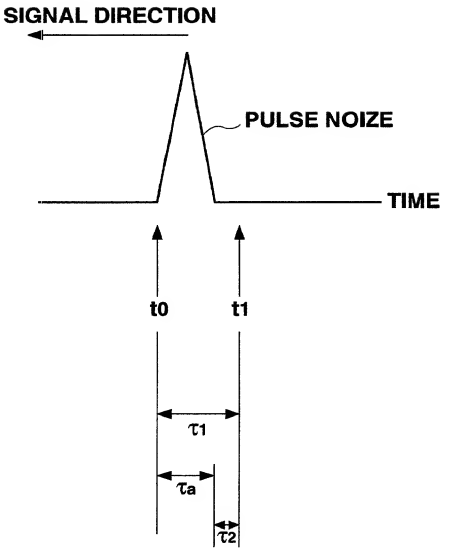


Fig. 6

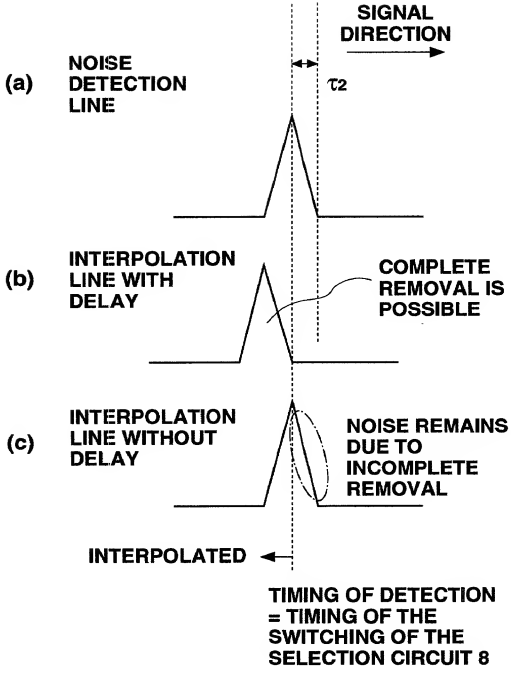
SIGNAL DIRECTION
(a)
NOISE DETECTION LINE
τ2
(b)
INTERPOLATION LINE WITH DELAY
COMPLETE REMOVAL IS POSSIBLE
(c)
INTERPOLATION LINE WITHOUT DELAY
NOISE REMAINS DUE TO INCOMPLETE REMOVAL
INTERPOLATED
TIMING OF DETECTION = TIMING OF THE SWITCHING OF THE SELECTION CIRCUIT 8

Fig. 7